SNP746

Highly integrated tire pressure monitoring sensor with BLE

SNP746 Datasheet

Release version: Version 1.2

Release date: 2023-09-27

Consultation Information

For further information on technical support, delivery and prices, please call the national consultation hotline: *021-5061-0206*, or you can obtain relevant support by email *info@senasic.com*.

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Features

- **MCU and Memories**
  - Up to 64 MHz Arm Cortex M0+ core, include IO port interface & 8 MPU regions
  - Support Serial Wire Debug
  - Direct Memory Access Controller
  - Support Download by ICP interface
  - Support ICache
- **Storage**
  - Total 80KB RAM, includes 32KB normal RAM, 16KB exchange RAM, 2x16KB Ret. RAM, 4KB Cache RAM
  - 512KB program flash memory with ECC
- **Power Management**
  - Integrated Buck DC-DC Converter
  - Sleep mode which can maintain BLE links support Wake up by:
    - BLE Low Power Timer
    - RTCs
    - A dedicated Wakeup PAD
    - A dedicated Wakeup RF Receiver
  - Deep Sleep mode support Wake up by:
    - RTCs
    - A dedicated Wakeup PAD
  - 2xRTCs
  - 1xBLE Low Power Timer
  - 1xRSTN PAD
  - 1xWK PAD
  - Power on Reset & Brown out Reset
- **Clocks**
  - 16/32MHz Crystal Oscillator
  - 32 kHz Crystal Oscillator
  - 1/4/32/64kHz RC Oscillator
  - 16/4/2MHz RC Oscillator
  - DPLL up to 64MHz
- **BLE system**
  - 2.4G Bluetooth Low Energy mode version 5.1 compliant
  - Support up to 8 simultaneous hardware connections
  - Date Rate: 2M, 1M, 500K, 125Kbps
  - Programmable TX Output Power -20dbm~6dbm
  - Rx Sensitivity: -96dbm
  - TX Power:6.3mA@0dbm with DCDC
  - RX Power:5.5mA with DCDC
  - Build in RSSI function
  - Dedicated Link Layer Processor
  - AES-128 Processor
  - A dedicated Wakeup RF Receiver
- 16-bit analog-to-digital converter (ADC16)
- **Peripherals**
  - 1xUART modules
  - 1xI2C modules
  - 1xSPI modules
  - 7 GPIOs
  - 1xWatch Dog Timer
  - 1xTrue Random Number Generator
  - 1x32 bits CRC
- Package: LGA 24pins. 6.0mmx5.0mmx1.9mm

Applications

- Tire Pressure Monitor with BLE interface

Contents

List of Tables

1 Introduction

SNP746 is a Bluetooth Low Energy chip integrated with measurement circuits for Pressure Sensor and Accelerometer Sensor. It is designed for tire pressure monitoring system with very low power consumption while withstand harsh automotive environment. It can also be as nodes of In-Vehicle wireless network.

SNP746 consists of a 64MHz Arm Cortex M0+ core,80KB RAM and 512KB Flash.The main frequency supports 16MHz and 64MHz modes, and includes an ICache with dedicated 4KB RAM. SWD download mode is supported.

SNP746 supports the BLE 5.1 protocol, in which the 2.4G RF part can be used as a separate 2.4G transceiver to support data transmission in a user-defined format.

SNP746 integrates 16bit ADC. It also integrates a large number of peripherals, including I2C, UART, SPI, GPIO, RTC, Timer, etc.

On-chip Flash memory stores the customer specific application program code, the unique ID-number and the calibration data for the sensor. Additionally, the embedded library functions developed by SENASIC cover standard tasks used by the application.

Table 1-1 Order Information

Model	Pressure Range	Package	Ordering Number	Packing Option
SNP74601CLE	100 ~ 900	LGA24	SNP74601CLE	3000ea/Reel
SNP74602CLE	100 ~ 1900		SNP74602CLE	3000ea/Reel

2 Pin Description

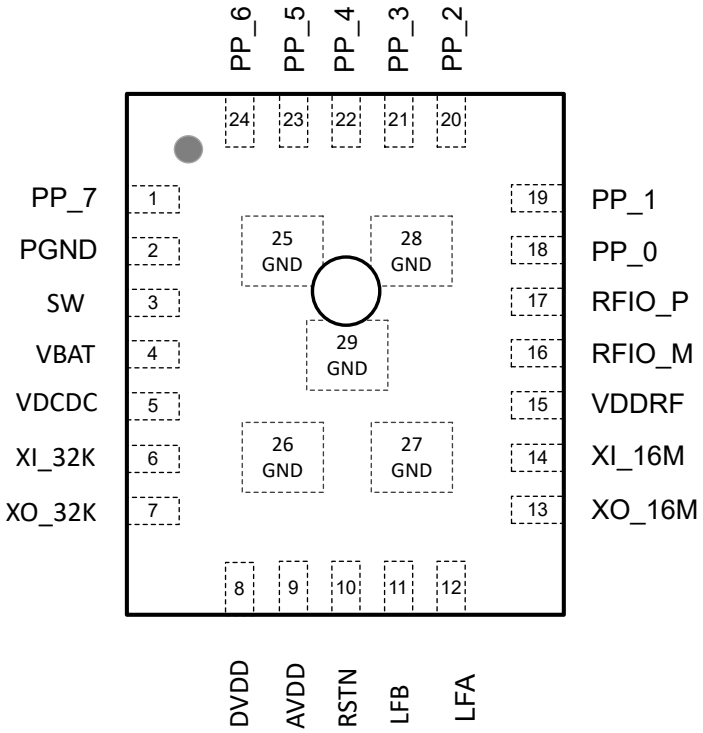


Figure 2-1 Pin Configuration(Top View)

Table 2-1 Pin Description

Pin No.	Name	Pin Type	Function
1	PP_7	DIO	ADC_3. INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset.
2	PGND	GND	Ground
3	SW	ANA	Switch regulator switching output
4	VBAT	PWR	Main power
5	VDCDC	PWR	1.8V Regulator output, decoupling cap needed
6	XI_32K	ANA	Crystal input for the 32 kHz XTAL
7	XO_32K	ANA	Crystal output for the 32 kHz XTAL
8	DVDD	PWR	Switch regulator output, decoupling cap needed
9	AVDD	PWR	0.9V Regulator output, decoupling cap needed
10	RSTN	DIO	Reset PIN, low active
11	LFB	Analog IO	LF channel coil connection
12	LFA	Analog IO	LF channel coil connection
13	XO_16M	ANA	Crystal output for the 16 MHz XTAL
14	XI_16M	ANA	Crystal input for the 16 MHz XTAL
15	VDDRF	PWR	RF Power supply input, decoupling cap need
16	RFIO_M	RF	RF Ground

Pin No.	Name	Pin Type	Function
17	RFIO_P	RF	RF antenna pin
18	PP_0	DIO	UART0_TX/I2C0_SCL/SPI_MOSI. INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset.
19	PP_1	DIO	UART0_RX/I2C0_SDA/SPI_CS. INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset.
20	PP_2	DIO	SWDIO
21	PP_3	DIO	SWDCLK
22	PP_4	DIO	ADC_0/UART1_TX/CAN_TX/SPI_SCK. INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset.
23	PP_5	DIO	ADC_1/UART1_RX/CAN_RX/SPI_MISO. INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset.
24	PP_6	DIO	ADC_2/INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset.
25~29	EPAD	GND	Ground

3 Specification

3.1 Absolute Maximum Ratings

Table 3-1 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Limiting supply voltage	V_{BAT_LIM}	-0.2		3.6	V	
Limiting voltage on a pin	V_{PIN_LIM}	-0.2		3.6	V	
Storage temperature	T_{STG}	-50		150	°C	
ESD HBM	V_{ESD_HBM}			2	kV	
ESD CDM	V_{ESD_CDM}	-750		750	V	
Latch-up current	I_{LAT}	-200		200	mA	T_A = 125°C

3.2 Operating conditions

3.2.1 Recommended Operating Conditions

Table 3-2 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Supply voltage	V_{BAT}	2.1		3.3	V	
Voltage on a pin	V_{PIN}	-0.2		V_{BAT}+0.2	V	
Ambient temperature	T_A	-40		125	°C	

3.2.2 Typical and maximum current consumption

Table 3-3 Typical and maximum current consumption

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
MCU Active Current	I_{MCU}		60		µA/ MHz	
Sleep Current 16KB Ret. RAM on	I_{SLP_16KRAM}			1.9	µA	
Sleep Current 32KB Ret. RAM on	I_{SLP_32KRAM}			2.5	µA	
Deep Sleep Current RTC on	I_{DSLP_RTC}			0.42	µA	@1kHz RTC
Deep Sleep Current RTC on, Wake up RF Receiver on	I_{DSLP_RF}			1.4	µA	1 second wake up latency
Flash Program Current	I_{FLASH_PROG}			3	mA	
Flash Erase Current	I_{FLASH_ERASE}			3	mA	

3.2.3 Internal clock source characteristics

Table 3-4 HFRC oscillator characteristics

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Frequency	f_{HFRC}		16		MHz	
user trimming step	TRIM		0.1		%	
Duty cycle			50		%	
Accuracy of the oscillator			1		%	T_A = -40 to 125°C
oscillator startup time	$t_{SU(HFRC)}$		6.8		μs	

Table 3-5 LFRC oscillator characteristics

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Frequency	f_{LFRC}		32		kHz	
user trimming step	TRIM		0.9		%	
Duty cycle			50		%	
Accuracy of the oscillator			10		%	T_A = -40 to 125°C
			2		%	T_A = 25°C
oscillator startup time	$t_{SU(LFRC)}$		2.5		ms	

3.2.4 Memory characteristics

Table 3-6 Flash memory characteristics

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Erase Time	t_{ERASE}			20	ms	For 10k Endurance
				100	ms	For 100k Endurance
Program Time	t_{prog}		4		ms	Every row, and a page is composed of 16 adjacent rows
Endurance	N_{END}	10k			cycles	Erase Time 20ms (max.)
		100k			cycles	Erase Time 100ms (max.)
Data retention	t_{RET}			10	years	
Supply current	I_{DD}			4	mA	Write mode
				6	mA	Erase mode
Programming voltage	V_{prog}			3.6	V	

3.2.5 I/O port characteristics

Table 3-7 I/O static characteristics

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Low level input voltage	V_{IL}			0.8	V	
High level input voltage	V_{IH}	2			V	
Input leakage current	I_{LKG}			15	μA	

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Weak pull-up equivalent resistor	R_{PU}	9		19.4	kΩ	
Weak pull-down equivalent resistor	R_{PD}	6.7		16	kΩ	
I/O pin input capacitance	C_{IN}		10		pF	
Output low level voltage for an I/O pin	V_{OL}			0.4	V	
Output high level voltage for an I/O pin	V_{OH}	2.4			V	
I/O pin output current	I_{IN}			15	mA	

Table 3-8 I/O AC characteristics

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Maximum frequency	$f_{max(IO)OUT}$		10		MHz	
Output fall time	$t_{f(IO)OUT}$			15	ns	
Output rise time	$t_{r(IO)OUT}$			10	ns	

3.2.6 Thermal Alarm circuit characteristics

Table 3-9 Thermal Alarm circuit characteristics

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Alarm Temp.	T_{ALARM}			125	°C	
Alarm release Temp.	T_{ALARM_RE}	95			°C	
Hysteresis	T_{HYST}		10		°C	

3.2.7 BLE RF characteristics

Table 3-10 BLE Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Operating frequency	f_{OPER}	2400		2480	MHz	
Number of channels	N_{CH}		40			
Channel frequency	f_{CH}		2402+K*2		MHz	K = 0 to 39

Table 3-11 BLE RF characteristics

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Rx Sensitivity			-96		dBm	1Mbps
Tx Output Power		-20		6	dBm	5dB/step
Supply current power down on VDDRF supplies	I_{PDN}				nA	
Supply current Tx On with PRF=0 dBm and DC-DC converter enabled	I_{BLE_TX0dBm}		6.3		mA	
RSSI accuracy		-2		+2	dBm	Over all temperature and frequency

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
BLE Rx Current with DC-DC converter enabled	I_{BLE_RX}		5.5		mA	
BLE Rx Current with DC-DC converter disabled	I_{BLE_RXb}		7		mA	

3.2.8 RF WAKE

Table 3-12 RF WAKE characteristics

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Sensitivity level	P_{SENS}	-40			dBm	
Current when RF WAKE Receiver is Active	I_{ACT}		2.2		μA	

4 Block Diagram

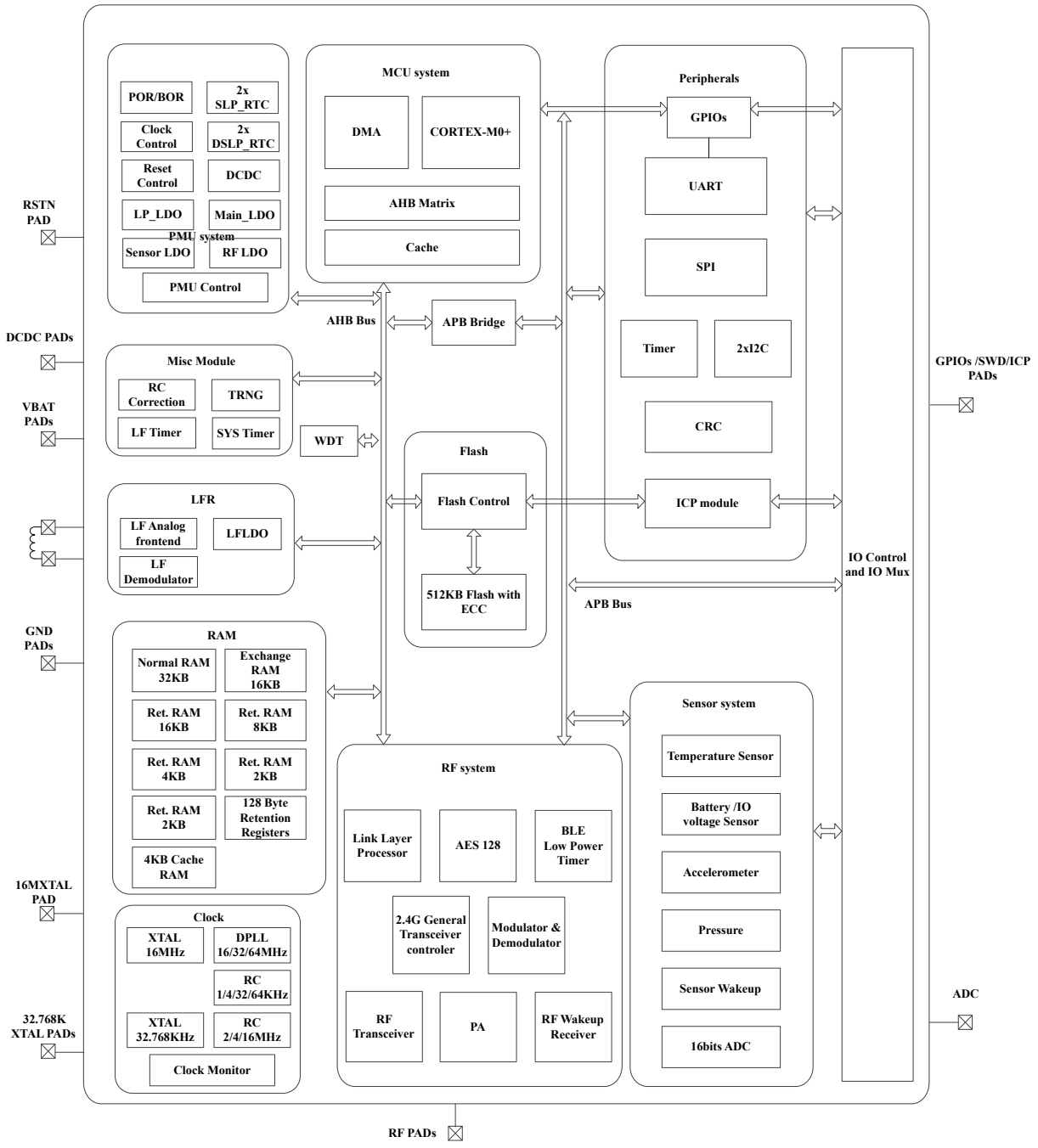


Figure 4-1 Block Diagram

5 Functional Description

5.1 MCU system

5.1.1 MCU

SNP746 has a Cortex-M0+ processor embedded whose performance up to 0.9 DMIPS/MHz with fast multiplier. It can run at system clock up to 64MHz and supports Serial Wire Debug.

Cortex-M0+ has a Built-in Nested Vectored Interrupt Controller and interrupts can have four different programmable priority levels and the NVIC automatically handles nested interrupts. It also includes a Sys-Tick timer.

The Cortex-M0+ used in SNP746 is configured to include IO port interface functionality for fast GPIO access. MPU functionality is also included and 8 regions can be configured for different access right. Up to 4 breakpoints are supported.

5.1.2 DMA

The Direct Memory Access (DMA) engine in SNP746 has 4 individual channels for fast transfer data between Peripherals, Sensor modules and RAMs.

Table 5-1 DMA Served Modules

NAME	Direction
UART	RX/TX
SPI	RX/TX
ADC in Sensor modules	RX

Note: DMA also supports transfer data between different RAM Regions.

5.1.3 Cache

When high performance is needed (MCU run above 16MHz), the Cache is needed. The Cache in SNP746 is an I-Cache. For Cache write operation, it adopts write through policy. For Cache read operation, it adopts Least Recently Used replacement policy.

5.2 RAM

SNP746 has total 80KB RAM. They are 32KB normal RAM, 16KB BLE Exchange RAM, two 16KB Retention RAMs, 4KB Cache RAM . All of them can be used by MCU, the Retention RAMs can retention data in sleep mode. If Cache function is not enabled, the corresponding RAM can also be used as normal RAM.

SNP746 also has 32 words retention registers which can keep value even in Deep Sleep mode.

5.3 Flash

The Flash in SNP746 is specially designed with high reliability for automotive applications. It is partitioned into two memory blocks: main block and information block.

The page erase operation erases all bytes within a page. A page is composed of 1024 words by 72 bits.The main block has 64 pages. The information block has 1 page and can be used for the storage of device information.

72-bit program proceeds with 36 consecutive bits of DIN as a group each time. When programming one group, set DIN bus to “1” in the rest group.

Table 5-2 Flash parameters

Parameter	Value	Comment
Erase Time	20ms	For 10K Endurance
	100ms	For 100K Endurance
Program Time	4ms	Every row, and a page is composed of 16 adjacent rows
Endurance	10K	Erase Time 20ms (max.)
	100K	Erase Time 100ms (max.)

5.4 PMU system

There are 3 power mode in SNP746, they are Active mode, Sleep mode and Deep Sleep mode. The status of the modules in these modes are shown in Table below.

Table 5-3 Module status in different power mode

Module	Active mode	Sleep mode	Deep Sleep mode
PMU system	√	√	√
32 words retention registers*	√	√	√
Wakeup RF Receiver	√	√	√
WK PAD and RSTN PAD	√	√	√
GPIO PADs*	√	√	√
LFRC	√	√	√
RAM (Retention RAMs) *	√	√	X
BLE low power timer	√	√	X
MCU system	√	X	X
RAM (normal RAM, Exchange RAM, Cache RAM)	√	X	X
Flash	√	X	X
Peripherals	√	X	X
IO control	√	X	X
Sensor system	√	X	X
BLE system (except Wakeup RF Receiver and BLE low power timer)	√	X	X
XTAL 16M & RC 16M	√	X	X

Note: Modules with * can only keep data/status in Sleep mode and Deep Sleep mode.

In Active mode, all the modules in SNP746 are power on. In Sleep mode, only the modules which are needed to maintain BLE link are power on. In Deep Sleep mode, only the modules used for regularly wake up are power on.

The wakeup methods of Sleep mode and Deep Sleep mode are shown in Table below.

Table 5-4 Wake up methods

Wake up methods	Sleep mode	Deep Sleep mode
RTCs	√	√
BLE Low Power Timer	√	x
WK PAD	√	√
Wakeup RF Receiver	√	√
RSTN PAD	√	√

Note: RSTN PAD can reset the chip and run into active mode, but the retention data are lost.

The power mode switch is realized in PMU control block by switch on/off the DCDC and LDOs.

The PMU control block works with the clock control block and reset control block to manage the clocks and resets in the chip. It also controls the retention of PADs.

There are two RTC in the PMU system. One is for RTC wake up purpose and the other is for Watch dog Timer purpose. Unlike the watch dog timer in Peripherals, the RTC realized watch dog timer is more reliable and can work in Sleep and Deep Sleep mode. When used as watch dog timer, RTC can generate interrupt or reset.

5.5 Clock

There are 2 Crystal Oscillator in SNP746, one is the 16 MHz Crystal Oscillator and another is the 32 kHz Crystal Oscillator. An external 16 MHz Crystal is needed for the 16 MHz Crystal Oscillator to generate the reference clock for the BLE RF circuit and DPLL. The external 32 kHz Crystal is used in BLE sleep mode.

SNP746 has two internal RC Oscillators, one is LFRC Oscillator and anther is HFRC Oscillator.

The LFRC Oscillator can be configured as 1/4/32/64 kHz and is used in Deep Sleep. It is also used as the always on clock to deal with the abnormal situations.

The HFRC Oscillator can be configured as 2/4/16 MHz and is used in situations when BLE is not needed. It is also used to deal with the abnormal situations.

There is an embedded DPLL in the chip to give the 64 MHz system clock.

5.6 BLE system

The BLE 5.1 system in SNP746 supports up to 8 simultaneous hardware connections, and can transmit and receive data at 2M, 1M, 500K, 125Kbps. The transmit output power is programmable and the receiver can give a RSSI indicator to show the energy strength of the signal. There is a hardware link layer processor to

relieve the MCU burden. A hardware AES-128 Processor is used for BLE security communication and it can also be used by custom applications.

The BLE low power timer works with 32 kHz Crystal Oscillator to wake up the chip from Sleep mode.

SNP746 has a dedicated Wakeup RF Receiver. It even works when the chip is in Deep Sleep mode. There are some parameters which help to make tradeoff between wakeup latency, false wakeup rate and average power consumption.

Table 5-5 BLE RF Parameters

Parameter	Value	Comment
Rx Sensitivity @ 1Mbps	-96dBm	
Tx Output Power	-20dBm to 6dBm	
RSSI accuracy	±2dBm	Over all temperature and frequency

5.7 Sensor system

The sensor system in SNP746 has a five-channel 16bit ADC, a Temperature Sensor, a Thermal Alarm circuit, a Pressure measurement circuit and an Accelerometer measurement circuit. It can be used to measure IO voltage (by 8 ADC input pads mux with GPIO support both differential and single ended input), Supply voltage, Temperature, Pressure and Accelerometer. With the Thermal Alarm circuit, an interrupt can be given out to indication extreme high temperature. Parameters in Sensor system is as follows.

Table 5-6 IO voltage sensor parameters

Parameter	Value	Comment
ADC ENOB	16	16 bits output
Sample Rate	3kHz	At 16 bits output

Table 5-7 Supply voltage sensor parameters

Parameter	Value	Comment
Measurement Range	From 2.1 to 3.6V	
Measurement Error	±3%	Percentage of measurement value

Table 5-8 Temperature sensor parameters

Parameter	Value	Comment
Temp. Precision	±3°C	From -40°C to 125°C
	±2°C	From -20°C to 70°C

Table 5-9 Thermal Alarm circuit parameters

Parameter	Value	Comment
Alarm Temp.	125°C	Max.
Alarm release Temp.	95°C	Min.
Hysteresis	10°C	Typ.

Table 5-10 Pressure sensor parameters @ max 900kPa

Parameter	Value	Comment
Input Range	100 to 900 kPa	
Resolution	1.1kPa/LSB	

Parameter	Value	Comment
Random Error	±2.3kPa	95% of all measurements
Measurement Error	±5kPa	0°C to 70°C, input range 100 to 500kPa
	±10kPa	-40°C to 0°C and 70°C to 125°C, input range 100 to 500kPa
	±7kPa	0°C to 70°C, input range 500 to 900kPa
	±15kPa	-40°C to 0°C and 70°C to 125°C, input range 500 to 900kPa

Table 5-11 Pressure sensor parameters @ max 1900kPa

Parameter	Value	Comment
Input Range	100 to 1900kPa	
Resolution	1.6kPa/LSB	
Random Error	±3.3kPa	95% of all measurements
Measurement Error	±7kPa	0°C to 70°C, input range 100 to 500kPa
	±15kPa	-40°C to 0°C and 70°C to 125°C, input range 100 to 500kPa
	±12kPa	0°C to 70°C, input range 500 to 900kPa
	±25kPa	-40°C to 0°C and 70°C to 125°C, input range 500 to 900kPa
	±20kPa	0°C to 70°C, input range 900 to 1500kPa
	±40kPa	-40°C to 0°C and 70°C to 125°C, input range 900 to 1500kPa

5.8 LFR

The low-frequency receiver (LFR) is a very low-power, low-frequency, receiver system for short-range communication in BLE TPMS. The module allows an external coil to be connected to two dedicated differential input pins. In BLE TPMS systems a single coil may be oriented for optimal coupling between the receiver in the tire or wheel and a transmitter coil on the vehicle body or chassis.

This LFR system minimizes power consumption by allowing flexibility in choosing the ratio of on to off times and by turning off power to blocks of circuitry until they are needed during signal reception and protocol recognition. In addition, this LFR system can autonomously listen for valid LF signals, check for protocol and ID information so the main MCU can remain in a very low power standby mode until valid message data has been received.

The LFR can be configured for various message protocols and telegrams to allow it to be used in a broad range of applications. The message preamble must be a series of Manchester coded bits at the nominal 3.906kbps data rate. A synchronization pattern is used to mark the boundary between the preamble and the beginning of Manchester encoded information in the message body. The synchronization pattern is a non-Manchester specific TPMS pattern. Messages can optionally include none, an 8-bit or a 16- bit ID value. Messages may contain any number of data bytes with the end-of-message indicated by detecting an illegal Manchester bit at a data byte boundary.

It is not intended that LFR may be actively receiving/decoding LF signals while physical parameter measurements are being made; or during the time that the RFM may be actively powered up and/or transmitting RF data. The resulting interactions will degrade the accuracy of the LF detection.

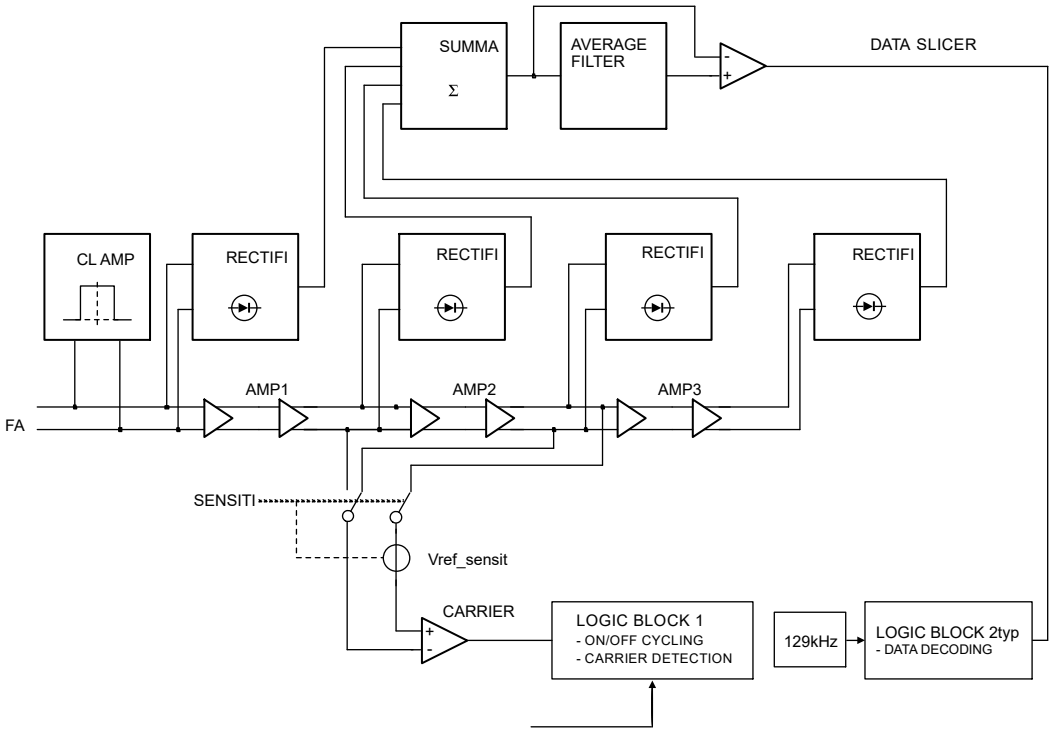


Figure 5-1 LFR Block Diagram

Design Scenarios for LFR: chip as the receiving passive party, in the master through the inductor transmission signal coupled to the chip when the chip in the 0.9v domain of the power-down situation, 3v domain of a low-power wireless wake-up mode, its carrier frequency 125KHz using ASK modulation. Main functions:

The LFR uses a timed-on mode where the off and on times are configurable by registers.

The common ratio of turn-on time to turn-off time is less than 1/10. to save power consumption, there are 2 phases before wake-up. The first stage is the carrier detection stage with only 1KHz clock; the second stage is the data reception stage with 125KHz clock for decoding the 3.9KHz baud rate data, and it will go back to the first stage if the decoding is unsuccessful.

The first stage: detects the threshold, frequency and carrier duration of the carrier within the opening window, and if the setting conditions are satisfied, it decides to enter the second stage (message wake-up mode) or wake up the CPU directly (carrier wake-up mode) according to the configured wake-up mode.

The second stage: data reception, which is divided into Manchester frame format and PWM frame format. Among them, Manchester frame format data baud rate is 3.9KHz, and it supports wake-up after matching to SYNC or wake-up after matching to WAKEID or wake-up after receiving 1byte data.

5.9 Peripherals

5.9.1 UART

They support 5/6/7/8 bits data length. The Stop bits can be set to 1/1.5/2bits. Parity is optional and Even Parity or Odd Parity are configurable. Each of them has 16 bytes RX FIFO and 16 bytes TX FIFO, and DMA is also supported.

5.9.2 I2C

There are two I2C interface in SNP746 which supports Standard mode (up to 100 kbits/s) and Fast mode (up to 400 kbits/s). They have 16 bytes RX FIFO and 16bytes TX FIFO and support 7-bit or 10-bit addressing, 7-bit or 10-bit combined format transfers.

5.9.3 SPI

There are two SPI interfaces in SNP746 which supports SPI mode 0, 1, 2 and 3 (clock edge and phase). They support 4-wire 8-bit SPI mode. Each of them has 32 bytes RX FIFO and 32 bytes TX FIFO, and DMA is also supported.

5.9.4 GPIO

There are 8 GPIOs in SNP746. four of them can also be used as ADC input for GPIO voltage measurement. There is configurable de-bounce logic for each I/O.

5.9.5 Watch Dog Timer

The watch dog timer in SNP746 can generate interrupt or reset, it is configurable whether to count down in IDLE. It cannot work in Sleep and Deep Sleep mode, use RTC in PMU system instead if needed.

5.9.6 Complicated Timer

There are eight 16-bit complicated timer in SNP746. All of them support Timer & Counter insertion functions.

5.9.7 TRNG

The True Random Number Generator in SNP746 can generate 32 bits random number in one microsecond.

5.9.8 CRC

The CRC32 module in SNP746 uses polynomial: 0x04C11DB7.

5.10 IO control

The IO control module deal with the IO mux and configuration of PADs (pull up, pull down, driver strength, IO mode selection, digital or analog IO). Input or output direction are indicated by IO mux and is determined by the assigned function.

6 Application Circuit

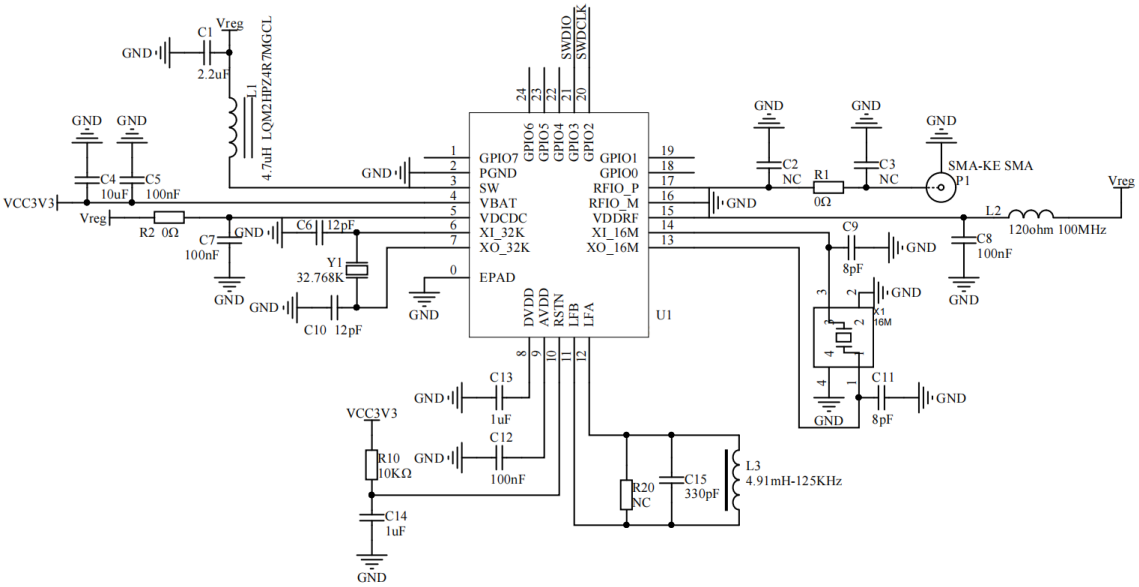
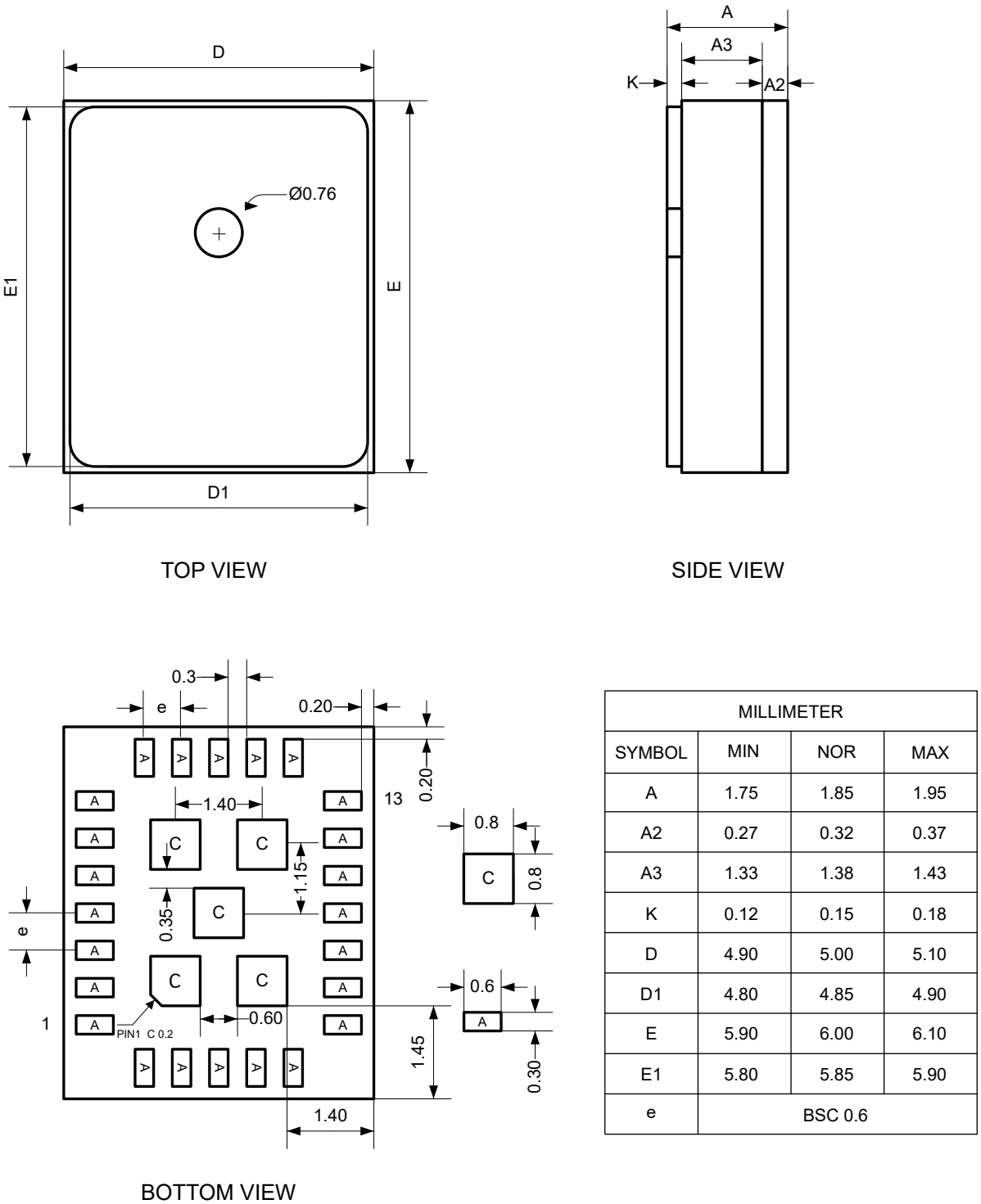


Figure 6-1 Application Circuit

7 Package Information

7.1 Package Outline



MILLIMETER			
SYMBOL	MIN	NOR	MAX
A	1.75	1.85	1.95
A2	0.27	0.32	0.37
A3	1.33	1.38	1.43
K	0.12	0.15	0.18
D	4.90	5.00	5.10
D1	4.80	4.85	4.90
E	5.90	6.00	6.10
E1	5.80	5.85	5.90
e	BSC 0.6		

Figure 7-1 Package Outline

7.2 Footprint

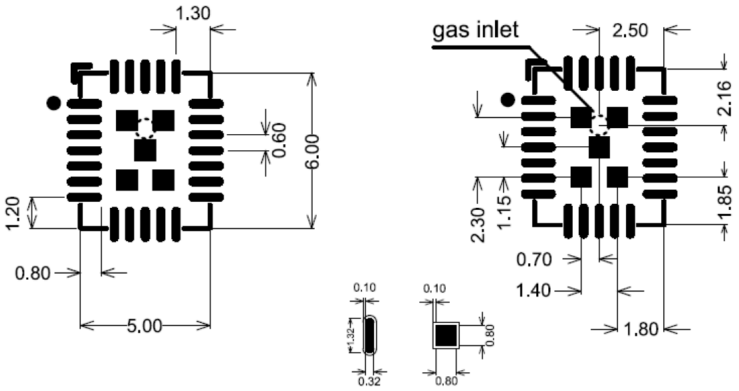


Figure 7-2 Recommend footprint layout

7.3 Marking

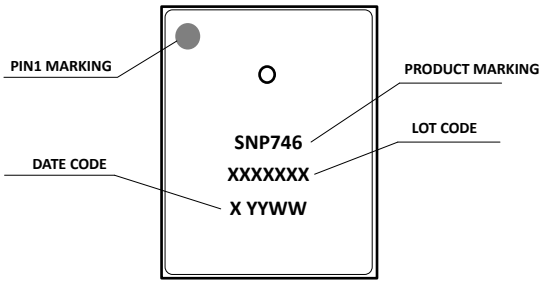


Figure 7-3 Marking information

Note: DATE CODE, YY representing year, WW representing week (When WW are “53”, means the 3th week of May).

7.4 Accelerometer

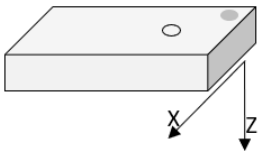


Figure 7-4 Acceleration sensor direction

8 Revision History

Table 8-1 Revision History

VERSION	DATE	NOTE
1.0	2023/08/11	Initial version.
1.1	2023/08/18	Modify some errors.
1.2	2023/09/27	Add functional description informations about LFR.