SNJ32W103

Arm® Cortex®-M0+ core, 80KB RAM, 512KB Flash, high performance, low power SOC with integrated Bluetooth communication

SNJ32W103 Datasheet

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Consultation Information

For further information on technical support, delivery and prices, please call the national consultation hotline: *021-5061-0206*, or you can obtain relevant support by email *info@senasic.com*.

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Description

The SNJ32W103 is a high-performance, low-power SOC that integrates Bluetooth LE communication. It contains an Arm® Cortex®-M0+ core, 80KB of RAM and 512KB of Flash. The main frequency supports two modes of 16MHz and 64MHz, and includes an ICache with a dedicated 4KB RAM. It Supports SWD download mode.

The chip supports BLE 5.1 protocol, in which the 2.4G RF part of the circuit can be used as a 2.4G transceiver alone, supporting data transmission in a customized format.

SNJ32W103 integrates a 16bit ADC. It also integrates a wealth of peripherals, including I2C, UART, SPI, CAN FD, LIN Flex, SENT, GPIO, RTC, Timer, etc. SPI, UART and LIN support DMA.

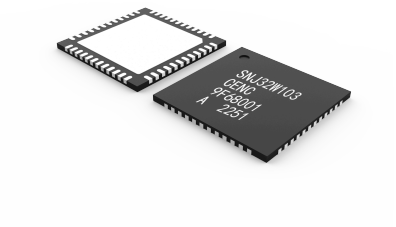
The chip supports Deep Sleep and Sleep mode. It meets the requirements of car standard. It is very suitable for vehicle intelligent wireless network.

Features

- MCU and Memories
  - Up to 64 MHz Arm Cortex M0+ core, include IO port interface & 8 MPU regions
  - Support Serial Wire Debug
  - Direct Memory Access Controller
  - 512KB program flash memory with ECC
  - 80KB RAM, includes 32KB normal RAM, 16KB exchange RAM, 2x16KB Ret. RAM
  - Dedicated RAM: 4KB Cache RAM and 1KB CAN RAM
- Power Management
  - Integrated Buck DC-DC Converter
  - Sleep mode which can maintain BLE links support Wake up by:
    - A dedicated BLE Timer
    - 4xRTCs
    - 4xWakeup PAD
    - A dedicated Wakeup RF Receiver
  - Deep Sleep mode support Wake up by:
    - 2xRTCs
    - 4xWakeup PAD
    - 4xRTCs
    - 1xBLE Low Power Timer
    - 1xRSTN PAD
    - 4xWK PAD
    - Power on Reset & Brown out Reset
- Clocks
  - 16/32 MHz Crystal Oscillator
  - 32.768 kHz Crystal Oscillator
  - 1/4/32/64 kHz RC Oscillator
  - 2/4/16 MHz RC Oscillator
  - 16/32/64 MHz DPLL
- BLE system
  - 2.4G Bluetooth Low Energy mode version 5.1 compliant
  - Support up to 8 simultaneous hardware connections
  - Date Rate: 2M, 1M, 500k, 125k bps
  - Programmable TX Output Power
  - Build in RSSI function
  - Dedicated Link Layer Processor
  - AES-128 Processor
  - A dedicated Wakeup BLE Timer
- 2.4G
  - Support customized data at the GFSK 2Mbit/s or 1Mbit/s data rate
  - A dedicated Wakeup RF Receiver
- Peripherals
  - 2xUART modules with LIN support
  - 2xI2C modules
  - 2xSPI modules
  - 1xCAN FD module
  - 1xSENT module
  - 32GPIOs
  - 1xWatch Dog Timer
  - 8xComplicated Timers which support:
    - Timer & Counter
    - PWM
    - Input Capture & Output Compare
    - Dead time insertion
  - 2xSimple Timer
  - 1xTrue Random Number Generator
  - 1x32 bits CRC
- Operating Characteristics
  - Voltage range: 1.8~3.6 V
  - Ambient temperature range: –40~125 °C

Application examples

- In-Vehicle wireless network
- Keyless entry/start (PEPS) system
- Tire pressure monitoring system (TPMS) controller
- AT command transparent transmission module
- Universal MCU (Combination of peripherals)



Order Information

Model	Package	Ordering Number	Packing Option
SNJ32W103	QFN48	SNJ32W103CENC	Tape & Reel

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1.1 Pin Configuration

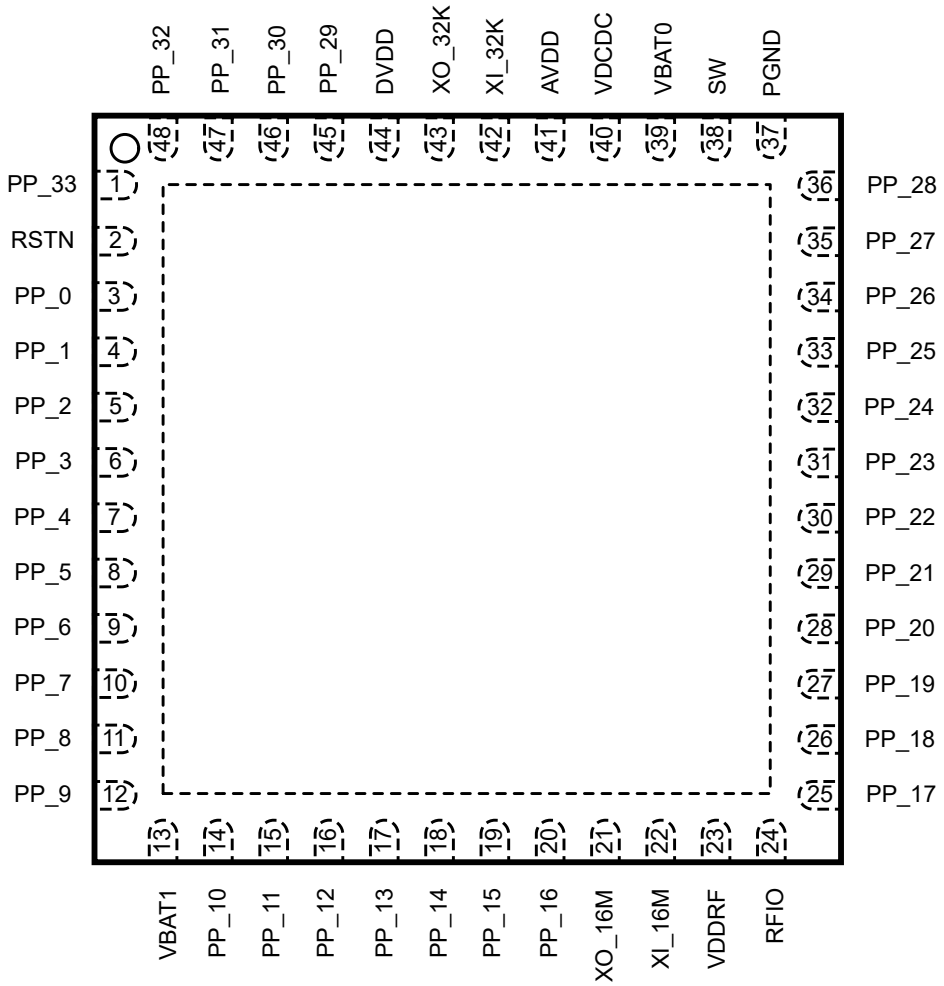


Figure 1-1 SNJ32W103 Pin Configuration

1.2 Pin Definition

Table 1-1 Pin Definition

Pin no.	Name	Type	Function
1	PP_33	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
2	RSTN	DI	INPUT. Reset PAD. Low vaild.
3	PP_0	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
4	PP_1	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
5	PP_2	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
6	PP_3	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
7	PP_4	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
8	PP_5	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
9	PP_6	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
10	PP_7	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
11	PP_8	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
12	PP_9	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
13	VBAT1	POWER	3V Power.
14	PP_10	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
15	PP_11	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
16	PP_12	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
17	PP_13	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
18	PP_14	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.

Pin no.	Name	Type	Function
19	PP_15	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
20	PP_16	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
21	XO_16M	AO	Crystal output for the 16 MHz XTAL.
22	XI_16M	AI	Crystal input for the 16 MHz XTAL.
23	VDDRF	POWER	RF Power.
24	RFIO	AIO	RF Output.
25	PP_17	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
26	PP_18	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
27	PP_19	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
28	PP_20	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
29	PP_21	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
30	PP_22	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
31	PP_23	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
32	PP_24	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
33	PP_25	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
34	PP_26	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
35	PP_27	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
36	PP_28	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
37	PGND	GROUND	Ground.
38	SW	POWER	DCDC Power. Connect to VDCDC with external Capacitor and Inductor.
39	VBAT0	POWER	3V Power for IOs & FLASH.
40	VDCDC	POWER	DCDC Power. Connect to SW.
41	AVDD	POWER	Anglog VDD.
42	XI_32K	AI	Crystal input for the 32.768 kHz XTAL.
43	XO_32K	AO	Crystal output for the 32.768 kHz XTAL.

Pin no.	Name	Type	Function
44	DVDD	POWER	Digital VDD. Connect to external Capacitor.
45	PP_29	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
46	PP_30	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
47	PP_31	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.
48	PP_32	DIO	INPUT/OUTPUT with selectable pull up/down resistors. Floating during and after reset. Contains state retention mechanism during Sleep and Deep Sleep mode.

Note: For details about pin reuse (IOMUX), see “SNJ32W103_Reference_Manual.pdf”.

2 Block Diagram

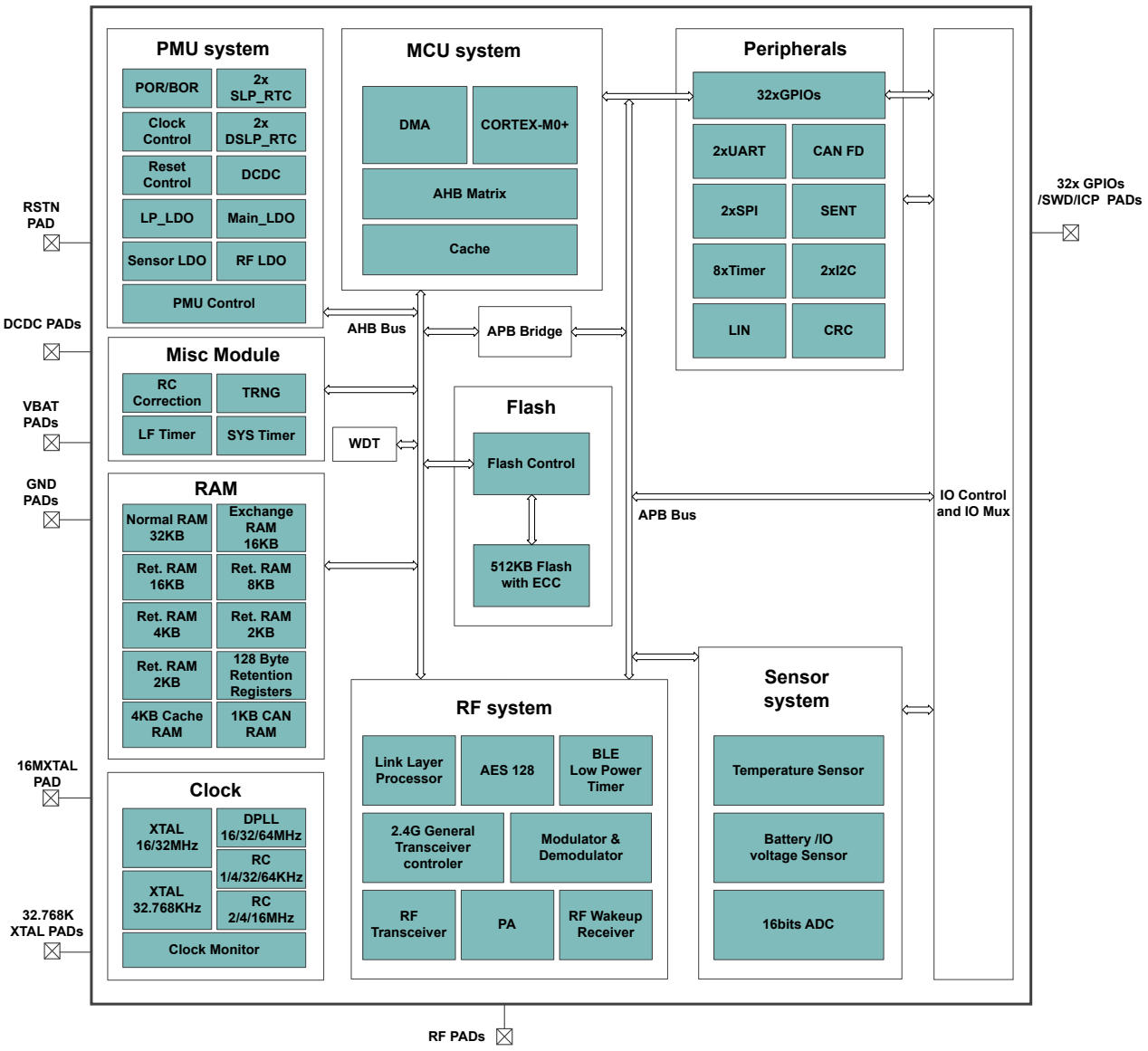


Figure 2-1 Block Diagram

3 Functional Description

3.1 MCU system

3.1.1 MCU

SNJ32W103 has a Arm Cortex-M0+ processor embedded whose performance up to 0.9 DMIPS/MHz with fast multiplier. It can run at system clock up to 64MHz and supports Serial Wire Debug.

Cortex-M0+ has a Built-in Nested Vectored Interrupt Controller and interrupts can have four different programmable priority levels and the NVIC automatically handles nested interrupts. It also includes a Sys-Tick timer.

The Cortex-M0+ used in SNJ32W103 is configured to include IO port interface functionality for fast GPIO access. MPU functionality is also included and 8 regions can be configured for different access right. Up to 4 breakpoints are supported.

3.1.2 DMA

The Direct Memory Access (DMA) engine in SNJ32W103 has 2 individual channels for fast transfer data.

Table 3-1 DMA Served Modules

Name	Direction
2xUART	RX/TX
2xSPI	RX/TX
LIN	RX/TX

Note: DMA also supports transfer data between different RAM Regions.

3.1.3 Cache

When high performance is needed (MCU run 64MHz), the Cache is needed. The Cache in SNJ32W103 is an I-Cache. For Cache write operation, it adopts write through policy. For Cache read operation, it adopts Least Recently Used replacement policy.

3.2 RAM

SNJ32W103 has 80KB RAM (Including 32KB normal RAM, 16KB BLE Exchange RAM, two 16KB Retention RAMs), 4KB Cache RAM and 1KB CAN RAM. The Retention RAMs can retain data in sleep mode. If Cache or CAN function is not enabled, the corresponding RAM can also be used as normal RAM.

SNJ32W103 also has 128 bytes retention registers which can keep value even in Deep Sleep mode.

3.3 Flash

The Flash in SNJ32W103 is specially designed with high reliability for automotive applications. It is partitioned into two memory blocks: main block and information block.

The page erase operation erases all bytes within a page. A page is composed of 1024 words by 72 bits.

The main block has 64 pages. The information block has 1 page and can be used for the storage of device information.

3.4 PMU system

There are 3 power mode in SNJ32W103, they are Active mode, Sleep mode and Deep Sleep mode. The status of the modules in these modes are shown in Table 3-2.

In Active mode, all the modules in SNJ32W103 are power on. In Sleep mode, the modules which are needed to maintain BLE link are power on. In Deep Sleep mode, the modules used for regularly wake up are power on.

The wakeup methods of Sleep mode and Deep Sleep mode are shown in Table 3-3.

The power mode switch is realized in PMU control block by switch on/off the DCDC and LDOs.

The PMU control block works with the clock control block and reset control block to manage the clocks and resets in the chip. It also controls the retention of PADs.

Table 3-2 Wake up methods

Module	Active mode	Sleep mode	Deep Sleep mode
PMU system	√	√	√
32 words retention registers*	√	√	√
Wakeup RF Receiver	√	√	√
WK PAD and RSTN PAD	√	√	√
GPIO PADs*	√	√	√
LFRC	√	√	√
RAM (Retention RAMs) *	√	√	×
BLE low power timer	√	√	×
XTAL 32.768kHz	√	√	×
MCU system	√	×	×
RAM (normal RAM, Exchange RAM, Cache RAM, CAN RAM)	√	×	×
Flash	√	×	×
Peripherals	√	×	×
IO control	√	×	×
Sensor system	√	×	×
BLE system (except Wakeup RF Receiver and BLE low power timer)	√	×	×
XTAL 16M & RC 16M	√	×	×

Note: modules with * can only keep data/status in Sleep mode and Deep Sleep mode.

Table 3-3 Wake up methods

Wake up methods	Sleep mode	Deep Sleep mode
RTCs	√	√
BLE Low Power Timer	√	×
WK PAD	√	√
Wakeup RF Receiver	√	×
RSTN PAD	√	√

Note: RSTN PAD can reset the chip and run into active mode, but the retention data are lost.

3.5 Clock

There are 2 Crystal Oscillator in SNJ32W103, one is the 16/32 MHz Crystal Oscillator and another is the 32.768 kHz Crystal Oscillator. An external 16/32 MHz Crystal is needed for the 16/32 MHz Crystal Oscillator to generate the reference clock for the BLE RF circuit and DPLL. The external 32.768 kHz Crystal is used in BLE sleep mode.

SNJ32W103 has two internal RC Oscillators, one is LFRC Oscillator and anther is HFRC Oscillator.

The LFRC Oscillator can be configured as 1k/4k/32k/64k Hz and is used in Deep Sleep. It is also used as the always on clock to deal with the abnormal situations.

The HFRC Oscillator can be configured as 2M/4M/16M Hz and is used in situations when BLE is not needed. It is also used to deal with the abnormal situations.

There is an embedded DPLL in the chip to give the 64MHz system clock.

3.6 BLE system

The BLE 5.1 system in SNJ32W103 supports up to 8 simultaneous hardware connections, and can transmit and receive data at 2M, 1M, 500k, 125k bps. The transmit output power is programmable and the receiver can give a RSSI indicator to show the energy strength of the signal. There is a hardware link layer processor to relieve the MCU burden. A hardware AES-128 Processor is used for BLE security communication and it can also be used by custom applications.

The BLE low power timer works with 32.768 kHz Crystal Oscillator to wake up the chip from Sleep mode.

SNJ32W103 has a dedicated Wakeup RF Receiver. It even works when the chip is in Deep Sleep mode. There are some parameters which help to make tradeoff between wakeup latency, false wakeup rate and average power consumption.

3.7 ADC & sensor system

SNJ32W103 has a eight-channel 16bit ADC, a Temperature Sensor and a Thermal Alarm circuit. It can be used to measure IO voltage (by 8 ADC input pads mux with GPIO support both differential and single ended input), Supply voltage, Temperature. With the Thermal Alarm circuit, an interrupt can be given out to indication extreme high temperature.

3.8 Peripherals

3.8.1 UART/LIN

There are two UART interface with LIN protocol support in SNJ32W103. They support 5/6/7/8 bits data length. The Stop bits can be set to 1/1.5/2 bits. Parity is optional and Even Parity or Odd Parity are configurable. Each of them has 16 bytes RX FIFO and 16 bytes TX FIFO, and DMA is also supported.

3.8.2 I2C

There are two I2C interface in SNJ32W103 which supports Standard mode (up to 100k bits/s), Fast mode (up to 400k bits/s), They have 8 bytes RX FIFO and 8 bytes TX FIFO and support 7-bit or 10-bit addressing, 7-bit or 10-bit combined format transfers.

3.8.3 SPI

There are two SPI interfaces in SNJ32W103 which supports SPI mode 0, 1, 2 and 3 (clock edge and phase). They support 3-wire 9bits and 4-wire 8bits SPI mode. Each of them has 32 bytes RX FIFO and 32 bytes TX FIFO, and DMA is also supported.

3.8.4 CAN FD

The FlexCAN module is a full implementation of the CAN protocol specification, the CAN with Flexible Data rate (CAN FD) protocol and the CAN 2.0 version B protocol, which supports both standard and extended message frames and long payloads up to 64 bytes transferred at faster rates up to 8 Mbps. The message buffers are stored in an embedded RAM dedicated to the FlexCAN module.

3.8.5 SENT

The SENT interface in SNJ32W103 is the full implement of the SAE J2716 protocol specification.

3.8.6 GPIO

There are 32 GPIOs in SNJ32W103. Eight of them can also be used as ADC input for GPIO voltage measurement. There is configurable de-bounce logic for each I/O.

3.8.7 Complicated Timer

There are eight 16-bit complicated timer in SNJ32W103. All of them support Timer & Counter, PWM, input Capture, output Compare and dead time insertion functions.

3.8.8 Watch Dog Timer

The watch dog timer in SNJ32W103 can generate interrupt or reset, it is configurable whether to count down in IDLE. It cannot work in Sleep and Deep Sleep mode, use RTC in PMU system instead if needed.

3.8.9 RTC

There are four RTC in the PMU system. They can be used as RTC wake up and Watch dog Timer. Unlike the watch dog timer in Peripherals, the RTC realized watch dog timer is more reliable and can work in Sleep and Deep Sleep mode. When used as watch dog timer, RTC can generate interrupt or reset.

3.8.10 TRNG

The True Random Number Generator in SNJ32W103 can generate 32 bits random number in one microsecond.

3.8.11 CRC

The CRC32 module in SNJ32W103 uses polynomial: 0x04C11DB7

3.9 IO control

The IO control module deal with the IO mux and configuration of PADs (pull up, pull down, driver strength, IO mode selection, digital or analog IO). Input or output direction are indicated by IO mux and is determined by the assigned function.

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4-1 Absolute Maximum Ratings

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Limiting supply voltage	V_{BAT_LIM}	-0.2		3.6	V	
Limiting voltage on a pin	V_{PIN_LIM}	-0.2		3.6	V	
Storage temperature	T_{STG}	-50		150	°C	
ESD HBM	V_{ESD_HBM}			2	kV	
ESD CDM	V_{ESD_CDM}	-750		750	V	
Latch-up current	I_{LAT}	-200		200	mA	T_A = 125°C

4.2 Operating conditions

4.2.1 Recommended Operating Conditions

Table 4-2 Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Supply voltage	V_{BAT}	1.8		3.3	V	
Voltage on a pin	V_{PIN}	-0.2		V_{BAT}+0.2	V	
Ambient temperature	T_A	-40		125	°C	

4.2.2 Typical and maximum current consumption

Table 4-3 Typical and maximum current consumption

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
MCU Active Current	I_{MCU}		60		µA/ MHz	
Sleep Current 16KB Ret. RAM on	I_{SLP_16KRAM}			1.9	µA	
Sleep Current 32KB Ret. RAM on	I_{SLP_32KRAM}			2.5	µA	
Deep Sleep Current RTC on	I_{DSLP_RTC}			0.42	µA	@1kHz RTC
Deep Sleep Current RTC on, Wake up RF Receiver on	I_{DSLP_RF}			1.4	µA	1 second wake up latency
Flash Program Current	I_{FLASH_PROG}			3	mA	
Flash Erase Current	I_{FLASH_ERASE}			3	mA	

4.2.3 Internal clock source characteristics

Table 4-4 HFRC oscillator characteristics

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Frequency	f_{HFRC}		16		MHz	
user trimming step	TRIM		0.1		%	
Duty cycle			50		%	
Accuracy of the oscillator			1		%	T_A = -40 to 125°C
oscillator startup time	$t_{SU(HFRC)}$		6.8		μs	

Table 4-5 LFRC oscillator characteristics

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Frequency	f_{LFRC}		32		kHz	
user trimming step	TRIM		0.9		%	
Duty cycle			50		%	
Accuracy of the oscillator			10		%	T_A = -40 to 125°C
			2		%	T_A = 25°C
oscillator startup time	$t_{SU(LFRC)}$		2.5		ms	

4.2.4 Memory characteristics

Table 4-6 Flash memory characteristics

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Erase Time	t_{ERASE}			20	ms	For 10k Endurance
				100	ms	For 100k Endurance
Program Time	t_{prog}		4		ms	Every row, and a page is composed of 16 adjacent rows
Endurance	N_{END}	10k			cycles	Erase Time 20ms (max.)
		100k			cycles	Erase Time 100ms (max.)
Data retention	t_{RET}			10	years	
Supply current	I_{DD}			4	mA	Write mode
				6	mA	Erase mode
Programming voltage	V_{prog}			3.6	V	

4.2.5 I/O port characteristics

Table 4-7 I/O static characteristics

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Low level input voltage	V_{IL}			0.8	V	
High level input voltage	V_{IH}	2			V	
Input leakage current	I_{LKG}				μA	
Weak pull-up equivalent resistor	R_{PU}	9		19.4	kΩ	

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Weak pull-down equivalent resistor	R_{PD}	6.7		16	kΩ	
I/O pin input capacitance	C_{IN}		10		pF	
Output low level voltage for an I/O pin	V_{OL}			0.4	V	
Output high level voltage for an I/O pin	V_{OH}	2.4			V	
I/O pin output current	I_{IN}			20	mA	

Table 4-8 I/O AC characteristics

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Maximum frequency	$f_{max(IO)OUT}$		10		MHz	
Output fall time	$t_{f(IO)OUT}$			15	ns	
Output rise time	$t_{r(IO)OUT}$			10	ns	

4.2.6 Thermal Alarm circuit characteristics

Table 4-9 Thermal Alarm circuit characteristics

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Alarm Temp.	T_{ALARM}			125	°C	
Alarm release Temp.	T_{ALARM_RE}	95			°C	
Hysteresis	T_{HYST}		10		°C	

4.2.7 BLE RF characteristics

Table 4-10 BLE Recommended Operating Conditions

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Operating frequency	f_{OPER}	2400		2480	MHz	
Number of channels	N_{CH}		40			
Channel frequency	f_{CH}		2402+ K*2		MHz	K = 0 to 39

Table 4-11 BLE RF characteristics

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Rx Sensitivity			-97		dBm	1Mbps
Tx Output Power		-20		6	dBm	5dB/step
Supply current power down on VDDRF supplies	I_{PDN}				nA	
Supply current Tx On with PRF=0 dBm and DC-DC converter enabled	I_{BLE_TX0dBm}		6.3		mA	
RSSI accuracy		-2		+2	dBm	Over all temperature and frequency

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
BLE Rx Current with DC-DC converter enabled	I_{BLE_RX}		5.5		mA	
BLE Rx Current with DC-DC converter disabled	I_{BLE_RXb}		7		mA	

4.2.8 RF WAKE

Table 4-12 RF WAKE characteristics

Parameter	Symbol	Values			Unit	Note
		Min.	Typ.	Max.		
Sensitivity level	P_{SENS}	-40			dBm	
Current when RF WAKE Receiver is Active	I_{ACT}		2.2		μA	

5 Application Circuit

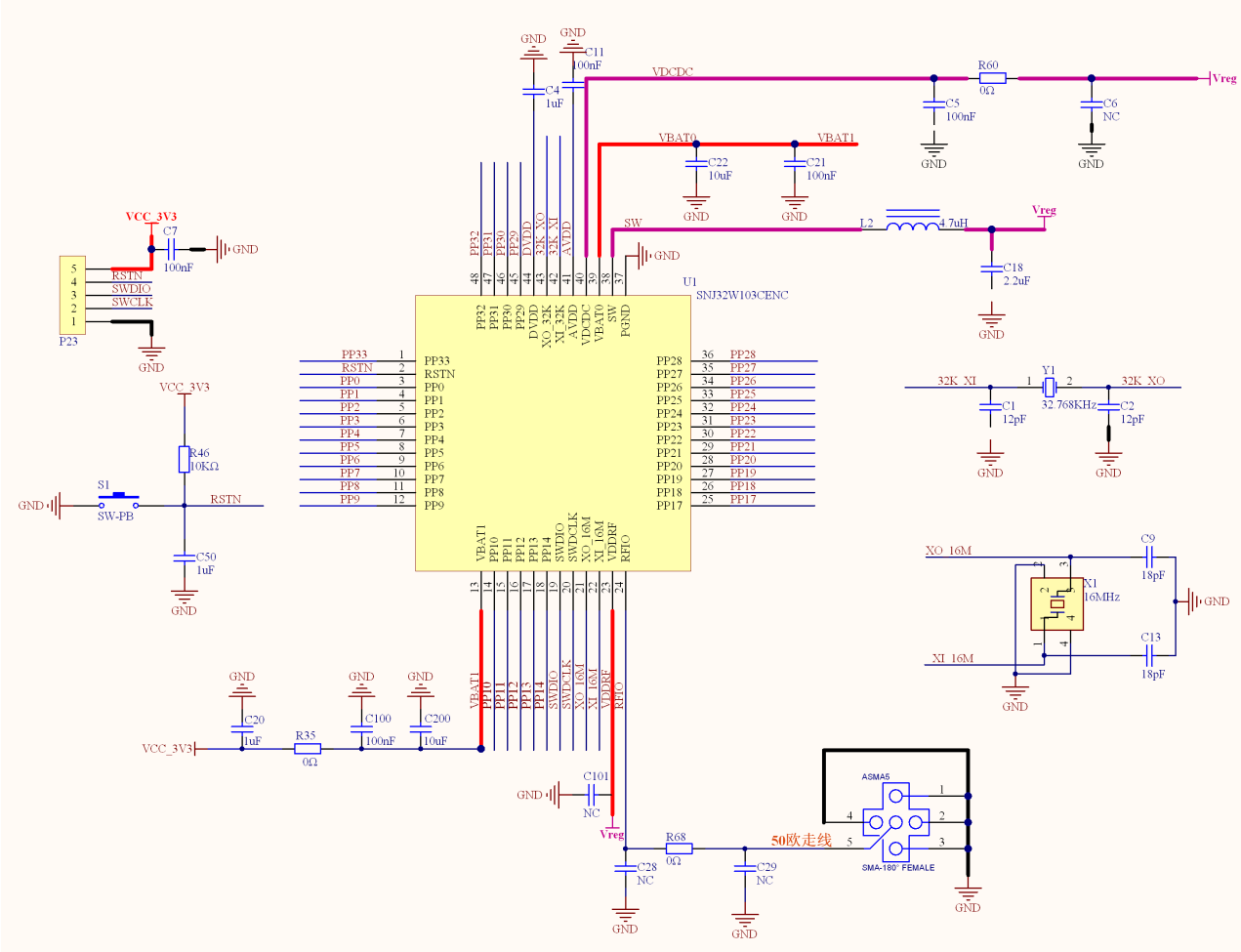
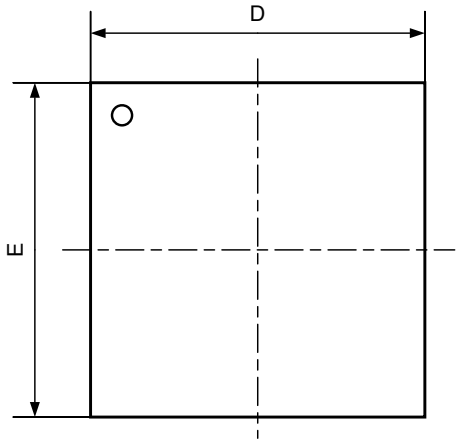
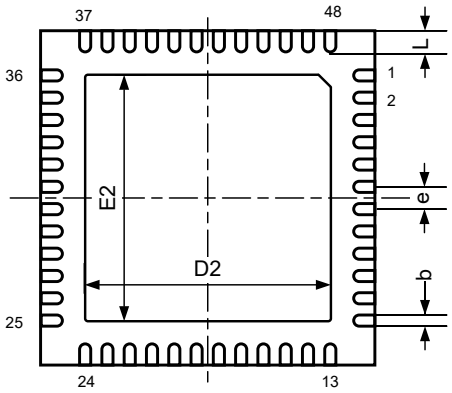


Figure 5-1 Reference Circuit for In-Vehicle wireless network application

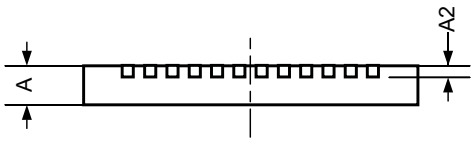
6 Outline Dimensions



TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Dimensions in Millimeters		
	Min	Nom	Max
A		0.750	
A2		0.203REF	
b	0.155	0.180	0.205
D		6.000	
E		6.000	
D2		4.300	
E2		4.300	
e	0.375	0.400	0.425
L	0.375	0.400	0.425

Figure 6-1 SNJ32W103 Package Dimensions

7 Revision History

Table 7-1 Revision History

VERSION	DATE	NOTE
V1.0	2023/8/11	Initial version